WHAT IS CLAIMED IS:

1 1. A method comprising the steps of:

2   determining a power mode for a device;

3   disabling a phase locked loop and providing an oscillator signal to drive a clock line when in

4   a first power mode; and

5   providing the oscillator signal to an input of the phase locked loop and providing a locked

6   signal from an output of the phase locked loop to the clock line when in a second

7   power mode.

1 2. The method as in Claim 1, wherein the device consumes less power in the first power mode than

2   in the second power mode.

1 3. The method as in Claim 1, further including the step of suspending processing within the device

2   when in a third power mode.

1 4. The method as in Claim 1, wherein the oscillator signal is generated through crystal oscillator.

1 5. The method as in Claim 1, wherein the oscillator signal is generated through an RC circuit.

1 6. The method as in Claim 1, wherein the output of the phase locked loop is coupled to a clock

2   divider and an output associated with the clock divider is coupled to the clock line.

1 7. The method as in Claim 6, wherein:

2   the step of disabling the phase locked loop, when in the first power mode, includes providing

3   the oscillator signal to the input of the clock divider; and

4   the step of providing the oscillator signal to the phase locked loop, when in the second

5   power mode, includes providing the locked signal to the input of the clock divider.

1 8. The method as in Claim 1, wherein the step of disabling the phase locked loop, when in the first

2   power mode, further includes providing reduced power, in comparison to an available power,

3   to the device.

1 9. The method as in Claim 1, wherein the step of disabling the phase locked loop, when in the first

2   power mode, further includes reducing, in comparison to a maximum number of bits used

3   available, a number of bits used to represent multimedia data.

1 10. The method as in Claim 9, wherein the multimedia data includes video data.

1 11. The method as in Claim 9, wherein the multimedia data includes audio data.

1 12. The method as in Claim 9, wherein the step of providing the oscillator signal to the phase

2   locked loop, when in the second power mode, further includes using the maximum number

3   of bits used to represent multimedia data.

1 13. The method as in Claim 1, wherein the device includes a portable device.

1 14. The method as in Claim 13, wherein the portable device includes a personal digital assistant.

1   15. The method as in Claim 1, wherein the step of providing the oscillator signal to the phase
2   locked loop, when in the first power mode, further includes reducing, in comparison to a
3   maximum number of bits used available, a number of bits used to represent multimedia data.

1   16. The method as in Claim 15, wherein multimedia data includes video data.

1   17. The method as in Claim 15, wherein multimedia data includes audio data.

1   18. The method as in Claim 15, wherein the step of disabling the phase locked loop, when in the
2   first power mode, further includes using the maximum number of bits used to represent the
3   multimedia data.

1   19. The method as in Claim 1, wherein disabling the phase locked loop includes shutting off power
2   used for driving the phase locked loop.

1   20. The method as in Claim 1, wherein providing the oscillator signal to drive a clock line includes
2   coupling a line carrying the oscillator signal to the clock line.

1   21. The method as in Claim 1, wherein the step of determining the power mode includes identifying
2   a number of pending instructions.

1   22. The method as in Claim 1, wherein the step of determining the power mode includes identifying
2   types of pending applications.

1   23. The method as in Claim 1, wherein the step of determining the power mode includes identifying
2   a change in display content.

1 24. A system comprising:

2 an oscillator having an input/output buffer, said oscillator to provide a source clock signal

3   using said input output buffer;

4 a phase locked loop having a first input/output buffer coupled to the input output buffer of

5   the oscillator, and a second input/output, said phase locked loop to provide a locked

6   clock signal;

7 a first multiplexor having a first input/output buffer coupled to the input/output buffer of the

8   oscillator, a second input/output buffer coupled to the second input output buffer of

9   the phase locked loop and a third input/output buffer, said multiplexor to:

10   when in a first power mode, pass said source clock signal to said third

11   input/output buffer; and

12   when in a second power mode, pass said locked clock signal to said third

13   input/output buffer;

14 a first clock line coupled to the third input/output buffer of the first multiplexor.

1 25. The system as in Claim 24 further including:

2 a second multiplexor having a first input/output buffer coupled to the input/output buffer of

3   the oscillator, a second input/output buffer coupled to the second input output buffer

4   of the phase locked loop and a third input/output buffer, said multiplexor to:

5   when in a first power mode, pass said source clock signal to said third

6   input/output buffer; and

7   when in a second power mode, pass said locked clock signal to said third

8   input/output buffer;

9 a second clock line coupled to the third input/output buffer of the second multiplexor.

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1   26. The system as in Claim 24, further including a first clock divider coupled between the first

2   multiplexor and the first clock line, said first clock divider to provide a divided clock signal

3   to the second clock line, wherein the divided clock signal is based on the locked clock signal,

4   when in the first power mode, and based on the source clock signal, when in the second

5   power mode.

1   27. The system as in Claim 24, wherein said oscillator includes a resister/capacitor circuit to

2   generate said source clock signal.

1   28. The system as in Claim 25, wherein said oscillator includes a crystal oscillator to generate said

2   source clock signal.

1   29. The system as in Claim 25, further including a power module, said power module to determine

2   a current power mode.

1   30. The system as in Claim 29, further including an instruction buffer to store instructions to be

2   processed.

1   31. The system as in Claim 30, wherein said power module determines said current power mode

2   based on the fullness of said instruction buffer.

1   32. The system as in Claim 30, wherein said power module determines said current power mode

2   based on a rate of change in a number of instructions in said instruction buffer.

1   33. The system as in Claim 30, wherein said power module determines said current power mode

2   based on types of instructions in said instruction buffer.

1   34. The system as in Claim 29, wherein said current power mode is based on a change in display

2   content.

1   35. The system as in Claim 24, wherein said first power mode is associated with a normal operation

2   mode and said second power mode is associated with a reduced power mode.

1 36. A computer readable medium tangibly embodying a program of instructions to manipulate a

2   system to:

3   determine a power mode for the system;

4   disable a phase locked loop and providing an oscillator signal to drive a clock line when in a

5   first power mode; and

6   provide the oscillator signal to an input of the phase locked loop and providing a locked

7   signal from an output of the phase locked loop to the clock line when in a second

8   power mode.

1 37. The computer readable medium as in Claim 36, wherein the system consumes less power in the

2   first power mode than in the second power mode.

1 38. The computer readable medium as in Claim 36, wherein the program of instructions is further

2   used to:

3   represent multimedia data using a first number of bits, when in the first power mode; and

4   represent multimedia data using a second number of bits, when in the second power mode,

5   wherein the first number of bits are less than the second number of bits.

1 39. The computer readable medium as in Claim 38, wherein the multimedia data includes video

2   data.

1 40. The computer readable medium as in Claim 38, wherein the multimedia data includes audio

2   data.

1 41. The computer readable medium as in Claim 36, wherein the power mode determined is based

2   on a number of pending instructions.

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1   42. The computer readable medium as in Claim 36, wherein the power mode determined is based

2   on a change in display content.

1   43. The computer readable medium as in Claim 36, wherein the power mode determined is based

2   on a type of instructions stored in the instruction buffer.